SM

Notice of Allowability	Application No. 10/709,370	Applicant(s) CHEN ET AL.	
	Examiner David Nhu	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *4/29/04*.

2. ☒ The allowed claim(s) is/are *1-16*.

3. ☒ The drawings filed on *29 April 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____.
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the change and/or additions be unaceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

Specifications:

Page 10, line 2, "couple voltage V_{cpuple} " should be –couple voltage V_{couple} --

Page 11, line 36, "couple voltage V_{cpuple} " should be –couple voltage V_{couple} --

Claims 1, 11, "ploysilicon" should be –polysilicon--

REASONS FOR ALLOWANCE

2. Claims 1-16 are allowed.

3. The following is an examiner's statement of reasons for allowance: None of the references of record teaches or suggests as cited in claims 1, 11: A method for programming a single-poly electrical programmable read only memory (EPROM) cell, said single-poly EPROM cell comprising a P-channel floating gate transistor on an isolated N-well of a P-type substrate, and an N-channel coupling device, wherein said P-channel floating gate transistor comprises P+ drain, P+source, P-channel defined between said P+ drain and P+source, tunnel oxide on said P-channel, and doped polysilicon floating gate on said tunnel oxide, and wherein said N-channel coupling device comprises a polysilicon floating agte electrode that is electrically connected to said doped polysilicon floating gate and is capacitively coupled to a control doped region formed in said P-type substrate, the method comprising: .. applying a positive voltage

on said control doped region so that said positive voltage being coupled to said P-doped polysilicon floating gate wherein said P-channel of said P-channel floating agte transistor is on "OFF" state, and a depletion region and electron-hole pairs are created at a junction between said P+ drain and said N well, and band-to-band tunneling (BTBT) induced hot electrons will inject into said doped polysilicon floating gate by tunneling through said tunnel oxide (as cited in claim 1); A method for programming a single-poly electrical programmable read only memory (EPROM) cell, said single-poly EPROM cell comprising a P-channel floating gate transistor on an isolated N-well of a P-type substrate, and an N-channel coupling device, wherein said P-channel floating gate transistor comprises P+ drain, P+source, P-channel defined between said P+ drain and P+source, tunnel oxide on said P-channel, and doped polysilicon floating gate on said tunnel oxide, and wherein said N-channel coupling device comprises a polysilicon floating agte electrode that is electrically connected to said doped polysilicon floating gate and is capacitively coupled to a control doped region formed in said P-type substrate, the method comprising: applying a negative voltage of –Vcc to said P+drain of said P-channel floating agte transistor; applying a parasitic BJT turn-on voltage to said P+ source of said P-channel floating gate transistor; and applying a positive voltage of +Vcc to said control doped region so that said positive voltage of +Vcc being coupled to said doped polysilicon floating gate (as cited in claim 11).

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

CONCLUSION

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Merrill et al (6,509,606 B1): Single Poly EPROM Cell Having Smaller Size and Improved Data Retention Compatible with Advanced CMOS Process.

Hsu et al (6,808,169 B2): Non-Volatile Memory with Crown Electrode to Increase Capacitance Between Control Gate and Floating Gate.

6. Any inquiry concerning this communication on earlier communications from the examiner should be directed to David Nhu , (571)272-1792. The examiner can normally be reached on Monday-Friday from 7:30 AM to 5:00 PM.

The examiner's supervisor, David Nelms can be reached on (571)272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703)872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956

David Nhu

April 2nd, 2005

DAVID NHU
PRIMARY E